MSI-P560

PC/104 96-CHANNEL DIGITAL INPUT/OUTPUT CARD

PC/104 Embedded
Industrial Analog I/O Series

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DESCRIPTION

The MSI-P560 provides 96 TTL level input/output lines arranged in four 24-bit digital I/O groups. Each group emulates a 8255 PPI (programmable peripheral interface) operating in mode 0. Each group is divided into three 8-bit ports ports A, B and C. Ports A and B can be configured as 8-bit input or output. Port C can be configured in two groups of four as input or output. I/O is provided by two 50-pin connectors. The unit is an 8-bit stackthrough PC/104 with I/O mapped 16-bit addressing for which addresses A5 thru A15 are jumper selectable. Requires +5V only. The card outline is shown in Figure 1.

A. Card Addressing

The I/O-mapped card address is set by installing appropriate jumpers on JP1, pins 1 thru 22. An uninstalled jumper for a given address bit sets the bit to 1 (true) and

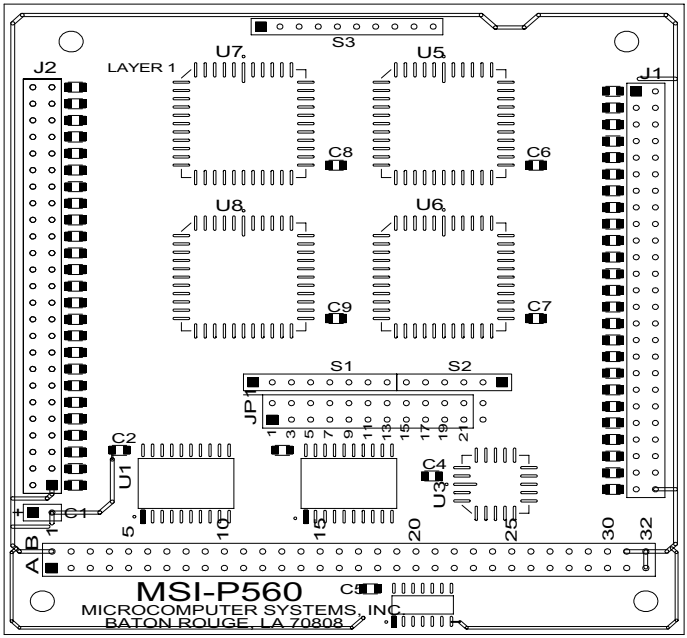

Figure 1. Outline of MSI-P560 Card.

an installed jumper sets the bit to 0 (false). Addresses A5 thru A15 are jumper selectable for defining the ***base address*** of the card from 0000H to FFE0H on integral 20H boundaries, where H denotes a hexadecimal number. To assign a base address of 300H, for example, install all jumpers except JP1-15,16 (A8) and JP1-13,14 (A9).

Individual channels have I/O addresses as given in Table 1 for the four 82C55A devices U5 thru U8.

Table 1. I/O Addresses of MSI-P460.

Channel	I/O Address *	Device	Connector
Port A0	base address	U5	J1, Pins 2-9**
Port B0	base address+1	U5	J1, Pins 10-17
Port C0	base address+2	U5	J1, Pins 18-25
Control0	base address+3	U5	
Port A1	base address+4	U6	J1, Pins 26-33
Port B1	base address+5	U6	J1, Pins 34-41
Port C1	base address+6	U6	J1, Pins 42-49
Control1	base address+7	U6	
Port A2	base address+8	U7	J2, Pins 49-42**
Port B2	base address+9	U7	J2, Pins 41-34
Port C2	base address+A	U7	J2, Pins 33-26
Control2	base address+B	U7	
Port A3	base address+C	U8	J2, Pins 25-18
Port B3	base address+D	U8	J2, Pins 17-10
Port C3	base address+E	U8	J2, Pins 9-2
Control3	base address+F	U8	

* Offsets from the base address are in hexadecimal notation.
** Pin 1 and 50 are ground.

B. Programming of the 82C55A PPI

A complete description of the 82C55A Programmable Peripheral Interface is available at

http://www.intersil.com/data/fn/fn2/fn2969/FN2969.pdf

C. Circuit Diagram of MSI-P560